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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,976	11/24/2003	Kyeong Keun Choi	29936/39768	5200

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,976	CHOI, KYEONG KEUN	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. Oath/Declaration filed on 11/24/03 has been considered.

Claim Objections

2. Claims 1, 2, and 6-8 are objected to because of informalities. Appropriate corrections are required to clarify scopes of the claim.

➢ With respect to claim 1,

line 13, "forming a metal line" should be changed to "forming the upper line" to clarify the scope of the claim.

➢ With respect to claim 2, the claim should be written in proper Markush group as below:

2. The method of claim 1, wherein the spacer insulating film is selected from a group consisting of a Si_3N_4 film and a SiC film, the spacer insulating film is stronger than that of the interlayer insulating film and is used as a metal diffusion barrier layer.

➢ With respect to claim 6, the claim should be written in proper Markush group as below:

6. The method of claim 1, wherein the interlayer insulating film is an oxide film having a low dielectric constant and formed by material selected from a group consisting of an spin-on-glass (SOG) film, an fluorine-doped tetra ethyl

ortho silicate (F-TEOS) film, a carbon doped dielectric (COD) film, and a porous low dielectric oxide film.

- With respect to claim 7,

line 8, "a via plug" should be changed to "the via plug" to clarify the scope of the claim.

- With respect to claim 8,

line 1, "wherein the step of forming the metal line" should be changed to "wherein the step of forming the upper line" to clarify the scope of the claim.

lines 3-4, "depositing a diffusion barrier film along a step difference of the semiconductor substrate on which the spacer is formed" should be changed to "depositing a diffusion barrier film along a step structure formed by the trench on which the spacer is formed" to clarify the scope of the claim.

line 8, "forming the metal line" should be changed to "forming the upper line" to clarify the scope of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. [US 6,452,274] in view of Ngo et al. [US 6,723,635].

➢ With respect to claim 1, Hasegawa et al. (figure 5's and cols 15-18) discloses a method for forming a metal line of a semiconductor device comprising steps of:

forming a via plug (58, figure 5D, col. 17 lines 22-23) on a semiconductor substrate (50, col. 16 lines 7-9);

forming an interlayer insulating film (59, figure 5E, col. 17 lines 24-28) on the semiconductor substrate (50) on which the via plug (58) is formed;

forming a trench by patterning the interlayer insulating film (col. 17 lines 42-48) in order to form an upper line (60, figure 5E, col. 17 lines 48-54); and

forming the upper line (60, figure 5E,col. 17 lines 42-54) by burying the trench with a conductive material.

Hasegawa et al. does not teach forming a spacer on a side wall of the trench by: depositing a spacer insulating film of which is more invulnerable to mechanical stress than the interlayer insulating film on the semiconductor substrate on which the trench is formed; and forming the spacer on the side wall of the trench by performing an anisotropic-dry-etching of the spacer insulating film.

However, Ngo et al teaches forming the spacer (20A, silicon carbide, figure 3, col. 5 lines 44-55 and col. 4 lines 8-18) by: depositing a spacer insulating film (20A, silicon carbide) on the semiconductor substrate on which the trench is formed (trench 16b, figures 1-2, col. 5 lines 5 lines 41-47); and forming the spacer (20A, figure 3) by

anisotropic-dry-etching (sputter etching, col. 5 lines 50-54: sputter etching is the anisotropic-dry-etching) the spacer insulating film. The advantage of forming the spacer of Ngo et al. is to protect the interlayer insulating film (15, col. 5 lines 7-24 & 38-40) from degradation during forming metal line in the trench (col. 4 lines 8-12 and col. 5 lines 20-24).

Therefore, at the time of invention, it would have been obvious for those skilled in the art, modify process of Hasegawa et al. by depositing the spacer insulating film and forming the spacer on the side wall of the trench as taught by Ngo et al. to prevent the interlayer insulating film from degradation when burying the trench with the conductive material. By combining the usage of spacer of Ngo et al (silicon carbide) in the process of Hasegawa et al. to prevent the interlayer insulating film from degradation, those skilled in the art would recognize that the spacer insulating film (silicon carbide) is more invulnerable to mechanic stress than the interlayer insulating film (low dielectric oxide film of porous silica xerogel). The claiming of a new use, new function or unknown property which is inherently present in the prior art (silicon carbide being more invulnerable to mechanical stress than the interlayer dielectric film of low dielectric oxide of porous silica xerogel) does not necessarily make the claim patentable. See In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977).

➢ With respect to claim 2, Ngo et al. (col. 3 lines 47-67, col. 4 lines 1-65 and col. 5 lines 20-67 and col. 6 lines 1-9) further discloses that the spacer insulating film is formed by a SiC film which has mechanical strength stronger than that of the insulating film (SiC has mechanical strength stronger than low k porous oxide, porous silica

xerogen) and is used as a metal diffusion barrier film (prevent barrier layer deposition inside the pores of the porous low k material). Therefore, at the time of invention, it would have been obvious for those skilled in the art to use the spacer insulating film as being claimed in the process of Hasegawa et al. in view of Ngo et al. to form metal interconnection of semiconductor device with reduced RC delay and without degradation of the interlayer insulating film (see Ngo et al., col. 2 lines 40-43, col. 3 lines 66-67, col. 4 lines 1-25 and col. 6 lines 16).

➢ With respect to claims 3-4, as being mention above, process of Hasegawa et al in view of Ngo et al substantially discloses the claimed process including depositing the spacer insulating film by using SiC. Ngo et al. also discloses depositing the spacer insulating film SiC with a thickness about 20-70Å (overlap with the claimed thickness) by PECVD at a temperature of 300-360°C (within the claimed temperature) under 2-4 torrs (within the claimed pressure). Therefore, at the time of invention, it would have been obvious for those skilled in the art to select the appropriate conditions for depositing the spacer insulating film SiC, as being claimed, in the process of Hasegawa et al. in view of Ngo et al. to provide effective protection to the interlayer insulating film from degradation. The claimed range parameters of depositing the spacer insulating film would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any

unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

➢ With respect to claim 6, both of Hasegawa et al. discloses the interlayer insulating film (59, figure 5E, col. 17 lines 24-28) is a porous low dielectric oxide film (porous silica of xerogel).

➢ With respect to claim 7, Hasegawa et al. (figures 5B-5E, col. 17) discloses the step of forming the via plug (58) comprising:

forming a lower line (54, figure 5B, col. 17 line 2) on the semiconductor substrate (50);

forming a second interlayer insulating film (57, figure 5C, col. 17 lines 6-8) on the semiconductor substrate (50), on which the lower line (54) is formed;

forming a via hole (figure 5D, col. 17 lines 19-23) by patterning the second interlayer insulating film in order to connect the lower line (54) with the upper line (60, figure 5E); and

forming the via plug (58, figure 5D, col. 17 lines 22-23) by burying the via hole with a conductive material.

➢ With respect to claim 8, as being mentioned above, process of Hasegawa et al in view of Ngo et al substantially discloses the claimed process including forming the spacer on the side wall of the trench and burying the trench with the conductive material. Ngo et al. (figure 4, col. 5 lines 57-65) further discloses forming metal line

(burying the trench with the conductive material) comprising: depositing a diffusion barrier film (barrier 40) along a step structure formed by the trench on which the spacer is formed; depositing a copper seed layer (41, col. 5 line 60) on the diffusion barrier layer; forming a copper film on the copper seed layer by electroplating method (col. 5 lines 64-65) thereby burying an opening portion; and forming the metal line by planarizing (CMP, col. 5 line 65) the copper film.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to form the upper line in the process of Hasegawa et al. in view of Ngo et al. by: depositing the diffusion barrier film along a step structure formed by the trench on which the spacer is formed; depositing the copper seed layer on the diffusion barrier film; forming the copper film on the copper seed layer by using electroplating method thereby burying the opening portion; and forming the upper line by planarizing the copper film. Since as taught by Ngo et al., such claimed steps of depositing the diffusion barrier film, depositing the copper seed layer, electroplating the copper film and planarizing the copper film have been known in the art of using damascene technology for forming metal line (see Ngo et al. col. 2 lines 12-22 and col. 5 lines 57-65). By using such claimed steps for forming the upper line in the process of Hasegawa et al. in view of Ngo et al., a metal interconnection will be formed with improved conductivity and low cost (see Ngo et al. col. 1 lines 63-67).

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al.[US 6,452,274] in view of Ngo et al. [US 6,723,635] as applied to claim 1 above, and further in view of Badih El-Kareh ["Fundamentals of

Semiconductor Processing Technology", Kluwer Academic Publishers: USA 1995, pp 296].

Hasegawa et al. in view of Ngo et al. substantially discloses the claimed method except teaching using reactive ion etching (RIE) for anisotropic-dry-etching the spacer.

However, Badih El-Kareh teaches that RIE is a known technique of anisotropic dry etching wherein etching rate can be improved by combination of physical and chemical process mechanism (see Badih El-Kareh page 296).

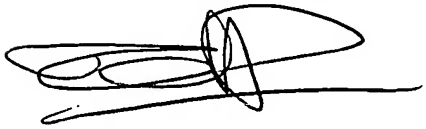
Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Hasegawa et al. in view of Ngo et al. by using the reactive ion etching as a known technique as taught by Badih El-Karel to dry etch the spacer insulating film anisotropically with high speed while maintaining a controlled profile of the etched spacer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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